CLAIMS

What is claimed is:

1.   An indicator mechanism for determining the validity of information communicated between two microprocessors using a dual port random access memory (RAM), comprising:

a sender for providing a data signal;

a dual port RAM for receiving said data signal from said sender,

said sender writing said data signal to a first memory location in said dual port RAM and an initialization status of said sender to a second memory location of said dual port RAM; and

a receiver for reading said initialization status of said sender from said second memory location of said dual port RAM, where said receiver subsequently reads said data signal from said first memory location of said dual port RAM in association with said initialization status of said sender.

2.   The mechanism of claim 1 wherein said initialization status is at least one of:

a prior-to-initialization state representing a state of said sender prior to an initialization of said dual port RAM;

an initialization-in-progress state representing a state of said sender being in progress of the initialization of said dual port RAM;

an initialization-complete state representing a state of said sender having completed the initialization of said dual port RAM; and

a power-down state representing a state of said sender being in power-down mode.

3.   The mechanism of claim 2 wherein said receiver reads said data signal when said initialization status is in said initialization-complete state.

4.   The mechanism of claim 2 wherein said receiver uses a default value when said initialization status is in at least one of said prior-to-initialization state, said initialization-in-progress state and said power-down state.

5.   The mechanism of claim 1 wherein said dual port RAM is provided within a controller, wherein said controller provides synchronous and asynchronous data transfer between an engine digital core and a transmission digital core of a vehicle.

6.   The mechanism of claim 5 wherein said dual port RAM further comprises a first side adapted to control data transfer from said engine digital core to said transmission digital core of said vehicle, wherein said sender is said engine digital core and said receiver is said transmission digital core.

7.   The mechanism of claim 5 wherein said dual port RAM further comprises a first side adapted to control data transfer from said transmission digital core to said engine digital core of said vehicle, wherein said sender is said transmission digital core and said receiver is said engine digital core.

8.   An apparatus for determining the validity of a data signal communicated between two microprocessors by a dual port random access memory (RAM), comprising:

a sender for providing a data signal and an initialization status indicator;

a dual port RAM in communication with said sender for receiving said data signal and said initialization status indicator, said dual port RAM having a first memory location for storing said data signal and a second memory location for storing said initialization status indicator of said dual port RAM;

said sender performing initialization on said dual port RAM at a beginning of a data transfer cycle, wherein said data transfer cycle includes a plurality of data transfers from said sender to a receiver, said sender updating said initialization status indicator as said initialization progresses; and

said receiver in communication with said sender from wherein said receiver reads said initialization status of said sender from said second memory location, said receiver subsequently reading said data signal from said first memory location in association with said initialization status of said sender.

9.   The apparatus of claim 8 wherein said operation status is at least one of:

a prior-to-initialization state representing a state of said sender being prior to an initialization of said sender;

an initialization-in-progress state representing a state of said sender being in progress of the initialization of said sender;

an initialization-complete state representing a state of said sender having completed the initialization of said sender; and

a power-down state representing a state of said sender being in power-down mode.

10.   The apparatus of claim 9 wherein said receiver reads said data signal when said initialization status is in said initialization-complete state.

11.   The apparatus of claim 9 wherein said receiver uses a default value when said initialization status is in at least one of said prior-to-initialization state, said initialization-in-progress state and said power-down state.

12.   The apparatus of claim 8 wherein said dual port RAM is provided within a controller, wherein said controller provides synchronous and asynchronous data transfer between an engine digital core and a transmission digital core of a vehicle.

13.   The apparatus of claim 12 wherein said dual port RAM further comprises a first side adapted to control data transfer from said engine digital core to said transmission digital core of said vehicle, wherein said sender is said engine digital core and said receiver is said transmission digital core.

14.   The apparatus of claim 12 wherein said dual port RAM further comprises a first side adapted to control data transfer from said transmission digital core to said engine digital core of said vehicle, wherein said sender is said transmission digital core and said receiver is said engine digital core.

15.   A method of determining the validity of information communicated between two microprocessors using a dual port random access memory (RAM), comprising:

performing initialization on a dual port RAM by a sender at the beginning of a data transfer cycle, wherein said data transfer cycle includes a plurality of data transfers from said sender to a receiver;

simultaneously writing an initialization status by said sender to a first memory location of said dual port RAM, wherein said initialization status includes at least one of a prior-to-initialization state indicative of said sender being prior to an initialization of said sender, an initialization-in-progress state indicative of said sender being in progress of the initialization of said sender, an initialization-complete state indicative of said sender having completed the initialization of said sender, and a power-down state indicative of said sender being in power-down mode;

writing a data signal to a second memory location of said dual port RAM by said sender after the step of performing initialization;

reading said initialization status from said first memory location of said dual port RAM by a receiver, wherein said receiver is in communication with said dual port RAM; and

reading said data signal from said second memory location of said dual port RAM by said receiver when said initialization status is in said initialization-complete state, said receiver using a default value when said initialization status is in at least one of said prior-to-initialization state, said initialization-in-progress state and said power-down state.

16.   The method of claim 15 wherein said dual port RAM is provided within a controller which provides synchronous and asynchronous data transfer between an engine digital core and a transmission digital core of a vehicle.

17.   The method of claim 16 wherein said dual port RAM further comprises a first side adapted to control data transfer from said engine digital core to said transmission digital core of said vehicle, wherein said sender is said engine digital core and said receiver is said transmission digital core.

18.   The method of claim 16 wherein said dual port RAM further comprises a first side adapted to control data transfer from said transmission digital core to said engine digital core of said vehicle, wherein said sender is said transmission digital core and said receiver is said engine digital core.